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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,528	12/29/2000	Leslie E. Cline	42390P10231	8822

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EXAMINER	
CONNOLLY, MARK A	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,528	CLINE ET AL.	
	Examiner	Art Unit	
	Mark Connolly	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10 and 12-29* is/are rejected.

7)☒ Claim(s) *3 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 have been presented for examination.

2. The rejections are respectfully maintained and reproduced infra for applicant's convenience.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 4, 6-9, 12, 14-19, 21, 23-27 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita, Jap Pat No 09288527.

5. Referring to claim 1, Yamashita teaches the apparatus comprising:

a. a table to contain a plurality of entries, each entry including a frequency field and a voltage field [¶ 0014].

b. a register coupled to the table and having a selection field to select one of the plurality of entries. Although not explicitly taught, it is inherent that the register must exist in the Yamashita system. A frequency and voltage decision circuit selects from a table a compatible voltage and frequency on which the system should run [¶ 0006, 0009 and 0014]. In order to save this selection, the above register is required.

c. wherein each of the entries is to indicate an operationally permissible combination of frequency and voltage [¶ 0009].

6. Referring to claim 4, Yamashita teaches that the frequency is a processor frequency [¶ 0004].

7. Referring to claim 6, Yamashita teaches that the voltage is a processor voltage [¶ 0003-0004].

8. Referring to claim 7, although Yamashita does not explicitly teach the table being disposed in non-volatile memory, it is inherent that the table would be so that the contents would not be lost when the system is powered off.

9. Referring to claim 8, it is interpreted that the Yamashita system includes at least two entries because the system is making a selection and therefore would require more than one entry in order to necessitate that selection.

10. Referring to claim 9, Yamashita teaches the computer system comprising:

d. a clock generator to selectively output a clock signal at any of a plurality of selectable processor clock frequencies [¶ 0004].

e. a power supply to selectively output any of a plurality of selectable processor operating voltages [¶ 0009].

f. a table coupled to the clock generator and the power supply and containing a plurality of entries, each entry including a frequency field and a voltage field [¶ 0014].

g. a register coupled to the table and having a selection field to select one of the plurality of entries. Although not explicitly taught, it is inherent that the register must exist in the Yamashita system. A frequency and voltage decision circuit selects from a table a compatible voltage and frequency on which the system should run [¶ 0006, 0009 and 0014]. In order to save this selection, the above register is required.

h. wherein the entries are each to contain values in the frequency and voltage fields that represent an operationally permissible combination of frequency and voltage [¶ 0009].

11. Referring to claims 12 and 14-16, these are rejected on the same basis as set forth hereinabove.

12. Referring to claim 17, Yamashita teaches the method comprising:

i. writing into a selection field of a register. Although not explicitly taught, it is inherent that the register must exist in the Yamashita system. A frequency and voltage decision circuit selects from a table a compatible voltage and frequency on which the system should run [¶ 0006, 0009 and 0014]. In order to save this selection, it is required that the selection would need to be written into the above register.

j. using a content of the selection field to select one of a plurality of entries in a table, each entry having a frequency field and a voltage field containing indicators of operationally permissible values for frequency and voltage [¶ 0009].

13. Referring to claims 18 and 19, Yamashita teaches indicating a processor frequency and voltage [¶ 0014].

14. Referring to claim 21, Yamashita teaches that the selected frequency is the processor clock [¶ 0004].

15. Referring to claims 23 and 24, Yamashita teaches that the voltage is a processor voltage [¶ 0003-0004].

16. Referring to claim 25, Yamashita teaches selecting a frequency and voltage that produce a combination that is operable in the processor [¶ 0006 and 0009].

17. Referring to claims 26, 27 and 29, Yamashita teaches the method and therefore teaches the instructions stored on a machine-readable medium to be executed on a processor performing the method.

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 2, 5, 10, 13, 20, 22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita as applied to claims 1, 4, 6-9, 12, 14-19, 21, 23-27 and 29 above.

20. Referring to claim 2, although Yamashita teaches a register to select one of a plurality of entries, it is not explicitly taught that the register also has a limit field to specify how many entries are selectable. In summary, Yamashita does not explicitly teach a means to enable only certain entries. Yamashita does though explicitly teach that as a battery discharges, the clock frequency and/or voltage must be reduced [¶ 0020-0022]. This is because high voltage and high frequency operation becomes infeasible as supply power diminishes. Therefore it would have been obvious to one of ordinary skill in the art to include a limit field into the Yamashita system because it would provide a means for the system to limit the selectable entries to only those that are compatible with the current battery power supply.

21. Referring to claim 5, although Yamashita teaches providing data for specifying a frequency for a processor, the format of that frequency specifying data is not explicitly taught. It would have been obvious to provide a multiplier as to indicate a processor frequency because it

is well known in the art and common practice that processors typically operate at a faster rate than the system buses and processor frequencies are specified as a multiple of those internal bus clocks through a multiplier factor.

22. Referring to claims 10, 13, 20, 22 and 28, these are rejected on the same basis as set forth hereinabove.

Allowable Subject Matter

23. Claims 3 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

24. Applicant's arguments filed 6 December 2004 have been fully considered but they are not persuasive.

25. In the remarks, applicants argued in substance that (1) examiner admitted that Yamashita does not teach the claimed register and "a rejection under 35 USC 102 requires that every element in the claim be found in the single cited reference" [page 8 in the Remarks]. (2) "Using the contents of a register to select an entry from a table is quite different than using a register to save an entry that has already been selected" [page 8 in the Remarks].

In response to argument (1), the applicant is mistaken. The examiner stated that the claimed register was not explicity taught in Yamashita, which is quite different than not being taught at al. The register not explicitly being taught can still be inherently within the teachings of Yamashita. Furthermore, "...inherent disclosures of a prior art reference may be relied upon in the rejection of claims under 35 U.S.C. 102..." [See section 2112 of the MPEP].

In response to argument (2), the applicant has misinterpreted the examiners grounds of rejection. Never did the examiner rely upon the register storing a copy of the selection as is essentially suggested by the applicant, but rather the frequency and voltage decision circuit uses the register in order to select the entries from the table. More specifically, the selection from the frequency and voltage decision circuit is saved in the register, wherein the register contents are used to perform the actual selection from the table. In order to select entries from a table, a register containing an address or row and column number referring to the entries is required.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (571) 272-3666. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mark Connolly
Examiner
Art Unit 2115

mc
February 8, 2005

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100